PC03V
VMEbus Time Code Processor

User's Guide
April 1996

CHAPTER ONE
INTRODUCTION

1.0 GENERAL

The PC03V Time Code Processor Operation and Technical Manual provides the following information:

- General Introduction and Definition of Terms
- Installation and Setup Details
- Software Interface Details
- I/O Signal Information
- Theory of Operation
- Programming Examples
- Drawing Set

1.1 FUNCTIONAL DESCRIPTION

The PC03V is a double height VMEbus module designed to decode serial time code signals and provide additional capabilities not normally found on a single board time code reader. The principal performance characteristics are listed in Table 1-1. The PC03V Module is shown in Figure 1-1. The PC03V provides the following capabilities:

- Decodes commonly used time code formats: IRIG A, IRIG B, IRIG G, 2137, XR3, NASA 36.
- Allows zero latency access to decoded time.
- Provides microsecond resolution when decoding in real-time.
- Provides carrier resolution when decoding in non-real-time.
- Provides a programmable interval heartbeat interrupt.
- Provides 2 programmable time coincidence strobes and 1 interval gate output.
- Allows time capture via an external event trigger input.
- Functions as an A16:D16 slave with flexible interrupt capabilities.
- It's 256 byte block can be located on any 256 byte boundary in the VMEbus short address space.
- Provides both front panel and P2 I/O connections.
- Can drive the Datum Inc. PC26V LED display module with the decoded time.

Table 1-1: PC03V Performance Specifications

Item	Description
Time Code Reader	
Time Code Formats	IRIG A,B,G, XR3, 2137, NASA 36
Carrier Range	250 Hz to 500 kHz
Code Direction	Forward and Reverse
Modulation Ratio	3:1 to 6:1
Input Amplitude	500 mV to 10 Volts Peak-Peak
Input Impedance	> 10k Ohms
VMEbus Interface	
Standardization	Revision C.1 of the VMEbus Spec
Location Monitor	A16, AM Codes $29 and $2D
Address Space	256 contiguous bytes
Data Transfer	D16
Interrupter	D08(O), I(1-7), ROAK
Power	+5VDC @ 1.7 A +12VDC @ 100 mA -12VDC @ 100 mA
TTL Input Signals	
Event Trigger	TTL, Positive or Negative Edge Triggered, 50 ns min width, 1 us min period
TTL Output Signals	
Strobe #1	LSTTL, Active Hi or Lo, 1 clock wide
Strobe #2	LSTTL, Active Hi or Lo, 1 clock wide
Interval Gate	LSTTL, Active Hi or Lo
Interval Counter	LSTTL, Active Lo, 1 clock wide
PDC Signals	LSTTL

Table 1-2: Time Code Resolution

Format	Carrier Resolution	PLL Resolution
IRIG A	100 microseconds	
IRIG B	1 millisecond	
IRIG G	10 microseconds	
2137	1 millisecond	1 microsecond
XR3	4 milliseconds	not available
NASA 36	1 millisecond	1 microsecond

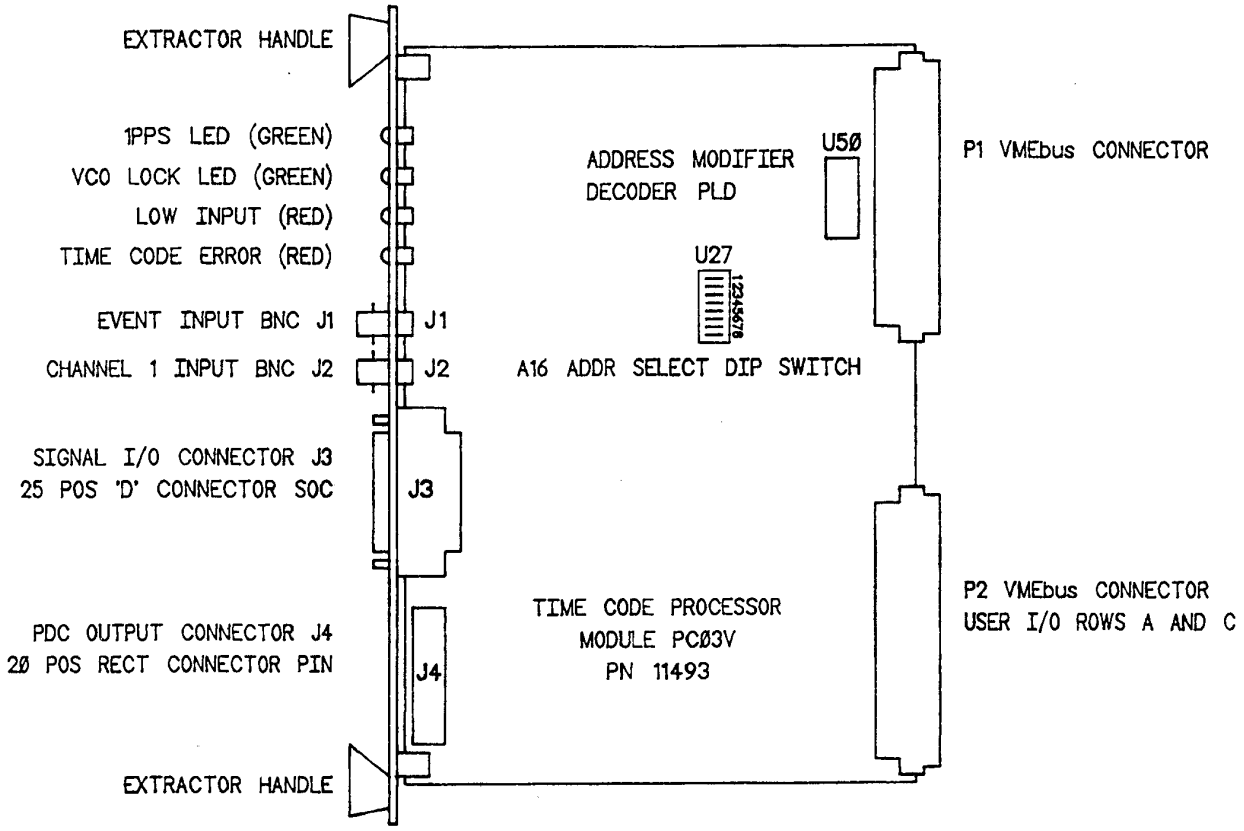


Figure 1-1: PC03V Module

1.2 TIME CODE FORMATS

The widespread use of coded timing signals to assist in the correlation of intercept and test data began in the early 1950's. These signals can be decoded in real time to indicate the current Time of Day (TOD) or recorded along with intercept/test data on magnetic tape recorders for post processing and time correlation.

Hundreds of time code formats were developed - one for each agency involved. During the early 1960's the InterRange Instrumentation Group promoted a series of 'standard' time code formats now loosely referred to as 'IRIG Time Codes'. The PC03V decodes three of these formats: IRIG A, IRIG B, and IRIG G.

Several other formats still enjoy relatively widespread use within their originating agencies: XR3, 2137, and NASA 36. These codes are also processed by the PC03V.

More complete details on these and other time code formats is available free of charge, on request from either Datum Inc. Division or Datum Inc in the form of the 'Datum Inc, Handbook of Time Code Formats'. Figure 1-2 illustrates a frame of IRIG A, B or G time code.

1.3 TIME CODE RESOLUTION

BCD encoded time of day is transmitted once per frame with an amplitude modulated signal. The PC03V Time Code Processor Module decodes the TOD data, once per frame, and counts the number of carrier cycles from the start of the frame, the 'on-time mark'. The PC03V also provides a phase-locked loop which converts the time code carrier into a 1 MHz clock which can be counted instead of the time code carrier. PC03V time resolution is therefore the period of the carrier or 1 microsecond (when the PLL clock is used at real-time rates.) Table 1-2 details the time resolution for each time code type when the carrier or 1 MHz PLL clock is used.

1.4 DEFINITION OF TERMS

A brief definition of the terms used throughout this manual is provided.

1PPS - 1 Pulse Per Second. A 1 carrier cycle wide pulse whose low to high going edge occurs on-time.

CAPTURE - The action of latching the current time and holding this time so that it can be read over the VMEbus.

CARRIER - The sinusoidal signal which when amplitude modulated becomes a time code signal. For example, IRIG B uses a 1 kHz carrier.

CLOCK - The TTL signal used to clock the minor time (subsecond) counters on the PC03V module. This signal is either at the carrier rate of the input time code or 1 MHz.

EVENT TRIGGER - An input to the PC03V whose positive or negative edge can be used to capture time and/or generate an interrupt.

FORWARD - Denotes the direction of time code where time increases.

HEARTBEAT - A signal generated by the PC03V that repeats every N number of CLOCK counts where N is set by the user.

INTERVAL GATE - A signal generated by the PC03V that is asserted by Strobe #1 and cleared by Strobe #2.

LATENCY - The interval between when time is requested and when the time can be read over the bus.

MAJOR TIME - Hundreds of days through units of seconds.

MINOR TIME - Hundreds of milliseconds through units of microseconds.

ON-TIME - The point in the time code frame where the encoded time is true.

PLL - Phased Locked Loop. On the PC03V, the time code carrier is used in a PLL circuit to generate a 1 MHz clock when the time code is running at real-time rates.

REAL-TIME RATE - The time code rate at which the timecode data changes by 1 second for every 1

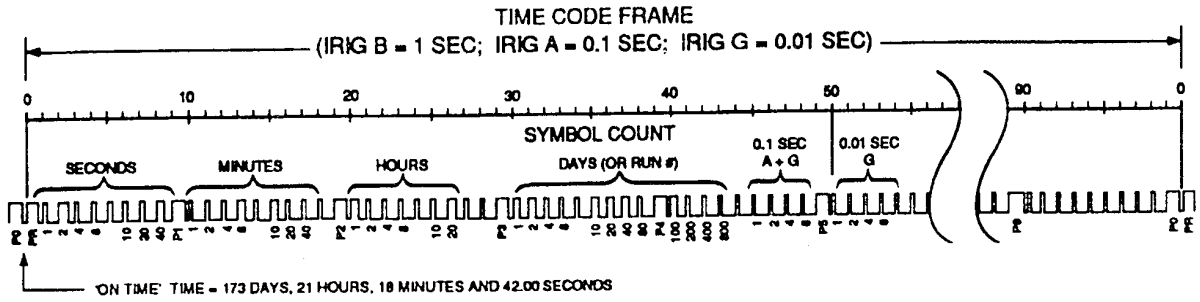
real-time second.

RESOLUTION - The least significant digit that can be read from the PC03V.

REVERSE - Denotes the direction of time code where time decreases.

STROBE - A signal generated by the PC03V which is active for one clock period and occurs at a specified time.

1a. Encoded Data. An IRIG B, 1-second frame period time code format is shown. For IRIG A, 0.1-second encoding is added where shown and for IRIG G, 0.01-second encoding is added.



1b. Symbols

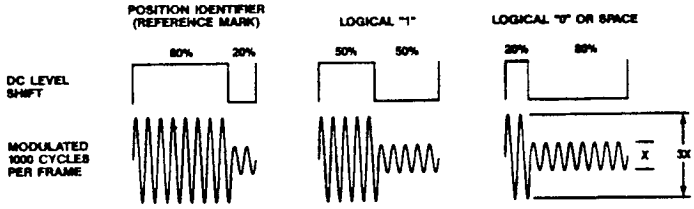


Figure 1-2: IRIG Time Code Format

CHAPTER TWO
INSTALLATION AND SETUP

2.0 GENERAL

The PC03V Time Code Processor Module is a double height VMEbus board designed to be installed in a standard VMEbus subrack. This section details the steps required to install the module in the subrack.

2.1 BASE ADDRESS SELECTION

Before installing the module in the subrack the address select DIP switch (U27) should be setup. The location of U27 is shown on Figure 1-1. The PC03V occupies 256 bytes in the VME short address space and can be freely located on any 256 byte boundary. The 8 DIP switch positions of U27 correspond to address bits A15-A8 as shown in Figure 2-1 and determine the base address for the module. The base address is defined as the address selected by the U27 DIP switch when A7-A1 are 0.

Dip Switch U27

Address Bit	A15	A14	A13	A12	A11	A10	A9	A8
U27 Switch	8	7	6	5	4	3	2	1

Figure 2-1: DIP Switch U27

To select a base address, set each of the 8 DIP switches to the ON (CLOSED) or OFF (OPEN) position. Setting a DIP switch to the ON position selects a logical 0 for that address bit, and the OFF position selects a logical 1.

The PC03V responds to address modifiers $2D (Short Supervisory Access) and $29 (Short Non-Privileged Access) as decoded by the U50 address modifier decoder PLD shown in Figure 1-1. This decoder PLD can be modified by the factory to decode different and/or additional address modifiers. Consult the factory for custom address modifier decoding.

2.2 INSTALLATION PROCEDURE

Once the base address has been selected the PC03V is ready to be installed in the VMEbus subrack. Install the PC03V as follows:

1. Remove the IACKIN*/IACKOUT* backplane jumper for the PC03V slot. This step should be done even if you will not be using interrupts from the PC03V.

2. Verify that your system does not utilize signals on rows A and C of the P2/J2 connector for VSB or other signals since the PC03V provides user I/O on these pins. If your system does have a P2/J2 conflict with the PC03V then you need a PC03V module which does not have the P2 connector installed.

3. Verify that the power to the subrack is turned off before inserting the PC03V module into the subrack.

4. Insert the PC03V into the subrack slot and secure the board in this slot by tightening the 2 front panel screws.

CHAPTER THREE
SOFTWARE INTERFACE

3.0 GENERAL

The PC03V occupies 256 bytes in the VMEbus short address space. Refer to Section 2.1 for details on base address selection. All data transfers between the VMEbus and the PC03V are D16 type (double-byte read and double-byte write). Some data transfers use only the lower byte (D0-D7) of the data lines, but must be implemented as D16 operations.

3.1 REGISTERS

This section describes the PC03V registers which control the capabilities of the module. Section 3.2 provides the details on how to use the registers to achieve the desired functions. The register model for the PC03V is listed in Table 3-1. The first column of this table shows the offset from the base address of each register. The column labeled 'R/W' shows whether the register is read-only (R), write-only (W), or read/writable (R/W). The notation 'A' in the R/W column indicates that a function occurs with either a read or write to that location, but that no transfer of data is defined. The data size is either a Word (D0-D15) or Byte (D0-D7) or undefined (--). The value of each register following a SYSRESET* is shown where '--' indicates the register contents is undefined. A label for each register is listed as is a brief description of the register's function.

3.1.1 CAPTR AND TIME0-3 REGISTERS

Accessing the CAPTR register with either a read or write causes the time (Days - Microseconds) to be loaded into a bank of latches which freezes the time at the instant the CAPTR register is accessed. Special circuitry prohibits the time from being latched while the time is changing. This circuitry is designed so that the user can read the time words immediately after an access to the CAPTR register without having to wait some predetermined amount of time (latency) for the time registers to become valid. This is referred to as zero latency time access.

A bank of 4 word (16-bit) registers holds the captured time. The time data is in a packed BCD format as shown in Table 3-2. The time is maintained in these registers until another CAPTR access takes place. An external event trigger or the programmable interval heartbeat pulse can also be used to capture time in the time registers (see Section 3.2).

PC03V REGISTER MODEL					
OFFSET HEX	R/W	DATA SIZE	RESET VALUE	LABEL	DESCRIPTION
00	A	--	--	CAPTR	Capture Time
02	R	W	--	TIME0	Time Word 0
04	R	W	--	TIME1	Time Word 1
06	R	W	--	TIME2	Time Word 2
08	R	--	--	TIME3	Time Word 3
0A	A	--	--	CLRIG	Clear Interval Gate
0C	R/W	B	00	CR0	Control Register 0
0E	R/W	W	00	CR1	Control Register 1
20	R/W	B	00	BIMCR0	BIM Control Register 0
22	R/W	B	00	BIMCR1	BIM Control Register 1
24	R/W	B	00	BIMCR2	BIM Control Register 2
26	R/W	B	00	BIMCR3	BIM Control Register 3
28	R/W	B	0F	BIMV0	BIM Vector Register 0
2A	R/W	B	0F	BIMV1	BIM Vector Register 1
2C	R/W	B	0F	BIMV2	BIM Vector Register 2
2E	R/W	B	0F	BIMV3	BIM Vector Register 3
30	A	--	--	RELFR	Release Capture Lockout
46-42	W	W	--	STR1W3-1	Strobe #1 (3 Registers)
66-62	W	W	--	STR2W3-1	Strobe #2 (3 Registers)
80	W	B	--	CTC0	CTC Counter 0 (Heartbeat)
82	W	B	--	CTC1	CTC Counter 1 (Not Used)
84	W	B	--	CTC2	CTC Counter 2 (Not Used)
86	W	B	--	CTCCR	CTC Control Register

Table 3-1: PC03V Register Model

TIME REG	D16 Data Bits (Packed BCD Format)			
	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
TIME0	status bits	days hunds	days tens	days units
TIME1	hours tens	hours units	minutes tens	minutes units
TIME2	seconds tens	seconds units	msec hunds	msec tens
TIME3	msec units	usec hunds	usec tens	usec units

TIME0 Status Bits (D15 - D12)	
BIT	Description
D15	Not Used (Always = 0)
D14	Low Input Signal 0 = Low
D13	1 MHz PLL Lock 0 = Locked
D12	Time Code Error 0 = Error

Table 3-2: Time Data Format (Packed BCD)

3.1.1.1 TIME STATUS BITS

The four most significant bits of TIME0 (D12-15) contain status information as listed in Table 3-2. The Time Code Error status bit (D12) will be 0 if an error occurred while reading time code. When a time code error is detected, the time data should be disregarded. Note that the time code error bit is valid only when a time code signal is present.

The Low Input Signal status bit (D14) will be 0 when the time code signal is either too low in amplitude or is not present. It takes approximately 2 to 3 seconds following loss of time code before the Low Signal status bit is activated.

The 1 MHz PLL Lock status bit (D13) will be 0 when the onboard 1 MHz Phase Locked Loop (PLL) is synchronized to the incoming time code. If this bit is 1 (unlocked) then the time code data read from the board should be disregarded.

3.1.2 CR0 AND CR1 CONTROL REGISTERS

The two control registers CR0 and CR1 control most of the functions on the PC03V. CR0 controls selection of the time code format, time code direction (fwd/rev), clock selection (carrier/PLL), and input

CR0 CONTROL REGISTER 0		
BIT	NAME	FUNCTION
0	TC0	TC2-0 Selects time code format 000 = IRIG B 001 = IRIG A 010 = IRIG G 011 = 2137 100 = XR3 101 = NASA 36 110 = Not Used 111 = Not Used
1	TC1	
2	TC2	
3	DIR	Time Code Direction 0 = Forward 1 = Reverse
4	CLOCK	Minor Time (Subsecond) Clock 0 = 1 MHz PLL 1 = Carrier
5	CHSEL0	CHSEL1-0 Selects Input Channel 00 = Channel 1 01 = Channel 2 10 = Channel 3 11 = Channel 4
6	CHSEL1	
7	---	Not Used

Table 3-3: CR0 Control Register 0

channel selection. CR1 controls the time coincidence strobes, external event trigger, heartbeat modes, and enables interrupts. Table 3-3 summarizes the function of the bits in CR0. Table 3-4 summarizes the function of the bits in CR1.

3.1.3 STR1W3-1 AND STR2W3-1 STROBE REGISTERS

The time coincidence strobe registers are write only and are used to hold the time of day data (Hours - Microseconds) for the 2 strobes. STR1W3-1 and STR2W3-1 are sets of 3 registers whose data format is identical to the packed BCD format for the TIME3-1 registers shown in Table 3-2. Note that Days are not used for the time coincidence strobes.

The sense (active low or high) of the 2 strobe outputs is controlled by ST1SENSE and ST2SENSE bits 10 and 11 of CR1. The mode (major/minor or minor only) of the 2 strobes is controlled by ST1MODE and ST2MODE bits 8 and 9 of CR1. The interval gate sense is controlled by IGSENSE bit 12 of CR1.

CR1 CONTROL REGISTER 1		
BIT	NAME	FUNCTION
0	FREN	Enable Secondary Capture Source 0 = Disable 1 = Enable
1	EVSENSE	Select Sense of Trigger Input 0 = Lo to Hi 1 = Hi to Lo
2	FRSEL	Select Secondary Capture Source 0 = Ext Event 1 = Enable
3	INTEN0	Interrupt Source 0 Int Enable 0 = Disable 1 = Enable
4	INTEN1	Interrupt Source 1 Int Enable 0 = Disable 1 = Enable
5	INTEN2	Interrupt Source 2 Int Enable 0 = Disable 1 = Enable
6	INTEN3	Interrupt Source 3 Int Enable 0 + Disable 1 = Enable
7	---	Not Used
8	ST1MODE	Strobe #1 Mode 0 = Major/Minor 1 = Minor Only
9	ST2MODE	Strobe #2 Mode 0 = Major/Minor 1 = Minor Only
10	ST1SENSE	Strobe #1 Output Sense 0 = Active High 1 = Active Low
11	ST2SENSE	Strobe #2 Output Sense 0 = Active High 1 = Active Low
12	IGSENSE	Interval Gate Sense 0 = Active High 1 = Active Low
13	HBSYNC	Sync Heartbeat to 1PPS 0 = No Sync 1 = Sync to 1PPS
14	---	Not Used
15	---	Not Used

Table 3-4: CR1 Control Register 1

PC03V Interrupt Sources	
INT	FUNCTION
0	External Event Trigger
1	Programmable Heartbeat Pulse
2	Time Coincidence Strobe #1
3	Time Coincidence Strobe #2

Table 3-5: Interrupt Sources

3.1.4 CTC0 AND CTCCR HEARTBEAT INTERVAL REGISTERS

The heartbeat interval pulse registers CTC0 and CTCCR are contained in an 82C54 Counter-Timer Chip (CTC). CTCCR is the control register for the chip and controls the mode for each of 3 16-bit counters contained on the chip. CTC0 is used to set the actual count for the heartbeat interval pulse. CTC1-2 are not used on the PC03V. The HBSYNC bit 13 of CR1 selects whether the counter is synchronized to the time code's 1PPS or free running (no sync).

3.1.5 CLRIG AND RELFR REGISTERS

The CLRIG register is used to clear the interval gate output. Any access to this register will immediately set the interval gate output to it's inactive state.

The RELFR register is used to release the time capture lockout that results when the secondary capture source is activated.

3.1.6 BIM REGISTERS

The Bus Interrupter Module (BIM) registers are contained in the Motorola MC68153. This IC provides VMEbus interrupt support for 4 interrupt sources. The 4 control registers (BIMCR0-3) govern the operation of the MC68153, and the 4 vector registers (BIMV0-3) contain the vector data used during an interrupt acknowledge cycle. MC68153 register bits 7-0 correspond to VMEbus data bits 7-0. When reading and writing to the MC68153 VMEbus data bits 8-15 are undefined.

The PC03V provides the 4 interrupt sources listed in Table 3-5. Interrupt source 0 (External Event Trigger) is governed by BIMCR0 and BIMV0 registers; interrupt source 1, by BIMCR1 and BIMV1; etc. Control Register 1 (CR1) bits 3-6 (INTEN0-3) must be set to a logical 1 to enable each interrupt as well. The BIMCR and BIMV registers should be configured before the CR1 INTEN bit is set to a logical 1.

3.1.6.1 INTERRUPT CONTROL REGISTERS

The Interrupt Control Registers govern the operation of the VMEbus interrupts. There is one control register for each interrupt source, i.e. BIMCR0 controls interrupt source 0, BIMCR1 controls interrupt source 1, etc. The Interrupt Control Register format is shown below.

BIT	7	6	5	4	3	2	1	0
FUNCTION	FLAG	FAC	X/IN	IRE	IRAC	L2	L1	L0

L2,L1,L0 - Interrupt Level
The 3 interrupt level bits determine the level at which an interrupt will be generated.

L2	L1	L0	IRQ LEVEL
0	0	0	DISABLED
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

IRAC - Interrupt Auto Clear
If the IRAC is set, IRE (Bit 4) is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing IRE disables the interrupt request. To re-enable the interrupt associated with this register, IRE must be set again by writing to the control register.

IRE - Interrupt Enable
This bit must be set to 1 to enable the bus interrupt request associated with the control register.

X/IN - External/Internal Vector
This bit must be cleared to 0 in all cases.

FAC - Flag Auto Clear
If FAC is set to 1, the FLAG bit is automatically cleared during an interrupt acknowledge cycle.

FLAG - Flag Bit
This bit is a flag that can be used for processor-to-processor communication and resource allocation. The FLAG bit has no affect on the operation of the interrupts.

3.1.6.2 INTERRUPT VECTOR REGISTERS

Each of the four interrupt sources has associated with it an interrupt vector register. Interrupt source 0 uses BIMV0, interrupt source 1 uses BIMV1, etc. The 8 bit interrupt vector is supplied to the VMEbus during an interrupt acknowledge cycle. The four Interrupt Vector Registers are set to 0F at reset which corresponds to the MC68000 vector for an uninitialized interrupt vector.

3.2 FUNCTIONAL DESCRIPTION

Section 3.1 provided an overview of the PC03V registers and their function. This section provides a description of how these registers are used to achieve the desired functions.

3.2.1 CAPTURING AND READING TIME

As described in Section 3.1.1, an access to the CAPTR register will freeze the current time, and this time will remain in the TIME3-0 registers until another capture takes place. Two other signals can also be setup to capture time. One source is the External Event Trigger Input. The Event input triggers the time capture on either it's low to high or high to low edge as determined by the EVSENSE bit (CR1 bit1). The other source of time capture is the programmable interval heartbeat pulse generated by the 82C54 Counter-Timer Chip (CTC). Only one auxiliary source (i.e. Event or Heartbeat) can be used for time capture at any given instant. The CAPTR register remains active while a secondary capture source is enabled. The FRSEL bit (CR1 bit 2) selects the secondary capture source, and the FREN bit (CR1 bit 0) enables the secondary capture source to capture time (NOTE: the secondary capture sources can always generate an interrupt even if the FREN bit is 0). When a secondary capture source freezes the time, the TIME3-0 registers will remain frozen until the RELFR register is accessed. That is, all capture sources (including the CAPTR register) will be locked out from capturing a new time. This precludes a capture source from overwriting the time registers before the user program has a chance to read them.

3.2.2 EXTERNAL EVENT TRIGGER

The External Event Trigger input provides a means of capturing time based on an event that occurs externally to the PC03V module. The EVSENSE bit (CR1 bit 1) controls which edge of this input is active. This input can also generate an interrupt (interrupt source 0) even if it is not enabled to capture time.

3.2.3 PROGRAMMABLE INTERVAL HEARTBEAT PULSE

The programmable interval heartbeat pulse can be used to generate a VMEbus interrupt and/or capture time. This active low heartbeat pulse is available on the I/O connectors. The heartbeat generator uses a 16-bit counter which counts either the time code carrier or 1 MHz PLL clock as determined by the CLOCK bit (CR0) bit 4. The CLOCK bit also determines the time resolution (See Section 3.2.6). The heartbeat pulse can be configured to be synchronized to the time code 1PPS or can free run as determined by the HBSYNC bit (CR1 bit 13).

SYSNC MODE	CTCCR	Interval
SYNC TO 1PPS (HBSYNC = 1)	$3A (HEX)	N + 1
FREE RUNNING (HBSYNC = 0)	#34 (HEX)	N

Table 3-6: CTCCR Control Byte

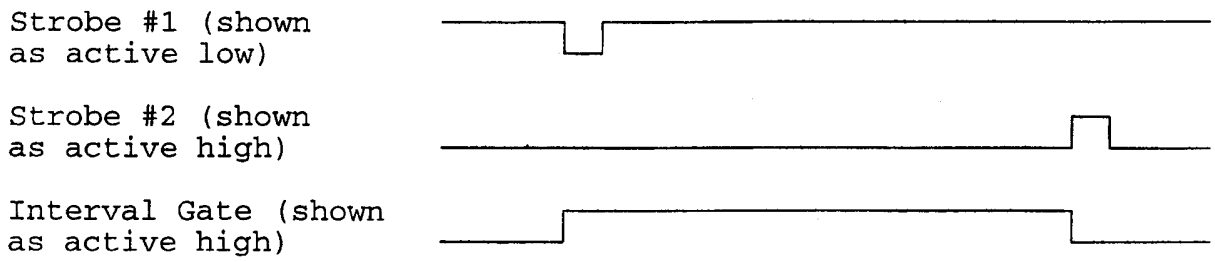
A control byte must be written to the CTCCR register before the two byte count is written to the CTC0 register. The value of the CTCCR control byte depends on whether the heartbeat is synchronized to the time code 1PPS or is free running. Table 3-6 lists the CTCCR control byte values used for both cases. This table also lists the heartbeat interval (number of clock cycles per pulse) for both cases.

The 16-bit count (N) is written to CTC0 as two consecutive bytes (D0-D7); least significant byte (LSB) first followed by the most significant byte (MSB). As shown in Table 3-6, the heartbeat will repeat every N+1 counts when synchronized to the 1PPS; when the heartbeat is free running, the heartbeat will repeat every N counts. (N = the count written into the CTC0 register.)

As described in Section 3.2.1 the heartbeat pulse can be used to capture time. The FREN bit (CR1 bit 0) enables the secondary capture source when set to 1, and the FRSEL bit (CR1 bit 2) selects the Heartbeat Interval Pulse as the secondary capture source when set to 1. The heartbeat pulse can also be used to generate an interrupt (interrupt source 1.) The heartbeat pulse can generate an interrupt even if it is not enabled to capture time.

3.2.4 TIME COINCIDENCE STROBES

Two time coincidence strobes, each of which produces a strobe 1 clock period wide, are provided. Each strobe is setup by loading 3 strobe registers (STR1W3-1 or STR2W3-1) with the time of day at which the strobe is to be activated. The format of the strobe data is the same as that shown in Table 3-2 (Days are not used.) STR1W1 corresponds to the TIME1 format, etc. The ST1SENSE and ST2SENSE bits (CR1 bits 10 and 11) determine the active sense of strobe #1 and strobe #2. All time digits (hours - microseconds) must be written into the registers. If the minor time clock source is the time code carrier then the less significant time digits must be set to 0. For example, if IRIG B is used and the CLOCK bit is set to 1 (carrier) then the three microsecond digits must be set to 0.



NOTE: Interval Gate transition occurs < 20 nsec after the strobe is activated

Figure 3-1: Strobes and Interval Gate Timing

Two modes of operation (major/minor and minor only) are implemented for each of the strobes. The ST1MODE and ST2MODE bits (CR1 bits 8 and 9) control the mode of operation for strobe #1 and strobe #2. The 'major/minor time' mode uses all time digits (hours tens - microseconds units) for time coincidence comparisons whereas the 'minor time only' mode uses only subsecond digits (milliseconds hundreds - microseconds units) for time coincidence comparisons. When using the 'minor time only' mode, the strobe will be activated once every second. The 'minor time only' mode ignores the hours tens - seconds units digits.

The Interval Gate signal is asserted when Strobe #1 is activated and is cleared when Strobe #2 is activated. The sense of the Interval Gate is controlled by the IGSENSE bit (CR1 bit 12). The Interval Gate is cleared by the SYSRESET* pulse, but can also be cleared by an access to the CLRIG register. Figure 3-1 shows the timing relationship between the two strobes and the interval gate. The two strobe pulses and the interval gate signals are available on the I/O connectors.

Each strobe can be used to generate an interrupt. Strobe #1 is interrupt source 2, and Strobe #2 is interrupt source 3. Again, to use the strobes as interrupts the BIM registers must be configured and the INTEN2 and INTEN3 control bits must be set to 1.

3.2.5 VMEbus INTERRUPTS

As described above, there are 4 sources of interrupts each of which functions independently. Each interrupt source can be configured to use any of the 7 (IRQ1-IRQ7) VMEbus interrupt levels or all 4 sources can use the same level if desired. Each source can also have a unique vector. The 4 interrupt enable bits in control register 2 (CR2) must be set to 1 to enable each interrupt source. These enable bits should be 0 until all other control bits and BIM registers are configured. All bits in the BIM control registers (BIMCR3-0) may be set as desired by the user except for bit 5 which must be cleared to 0 (internal interrupt response).

3.2.6 READING TIME AT DIFFERENT RESOLUTIONS

Table 1-2 shows the resolution of each time code format when the carrier is used to clock the minor time counters (CLOCK bit = 1). All less significant digits will be forced to 0 when using the carrier. For example, when reading IRIG B with the carrier clock, the 3 microsecond digits will always be read as 0.

XR3 is a special case because it's carrier frequency is only 250 Hz. The subsecond digits for XR3 will range from .000 to .249 each second. The XR3 subsecond digits must therefore be multiplied by 4 to produce the actual subsecond count. For example, when a subsecond value of .123 is read, the actual subsecond value is .492 (.492 = 4 X .123).

When using the PLL clock (CLOCK bit = 0) the time resolution will be 1 microsecond for all codes except XR3 which will not function with the PLL clock. The PLL clock can be used only at real-time rates. Using the PLL clock at nonreal-time rates will result in erroneous subsecond counts being read.

3.2.7 READING TIME IN REVERSE

When reading time that has been recorded on a magnetic tape recorder, it is possible to read the time in reverse (i.e time decreases). The subsecond counters, however, always count up. This means that the subsecond count read in reverse will be increasing instead of decreasing (the major time does decrease). For example, the value of the subsecond count following the on-time mark should be .999999, then .999998, etc., but will be read as .000000, .000001, etc. The minor time count must be converted by subtracting the count read from .999999.

Actual Minor Time = 0.999999 - Minor Time Read

CHAPTER FOUR
I/O CONNECTORS

4.0 GENERAL

All I/O signals are available on the VMEbus P2 connector on rows A and C. All I/O signals (except the PDC signals) are also available on the front panel 25 pin 'D' connector. The Channel 1 time code input and the Event Trigger input are also available on front panel BNC connectors. The PDC signals are available on a 20 pin rectangular connector located near the front panel. The location of all connectors is shown in Figure 1-1.

4.1 J1 EVENT TRIGGER INPUT

The Event Trigger Input is available on the front panel BNC labeled 'EVENT' and is connected in parallel with the other connectors which carry this signal.

4.2 J2 CHANNEL 1 TIME CODE INPUT

The Channel 1 time code input is available on the front panel BNC labeled 'CH 1' and is connected in parallel with the other connectors which carry this signal.

4.3 J3 SIGNAL I/O CONNECTOR

All I/O signals (except the PDC signals) are connected to the front panel 25 pin 'D' connector labeled 'J3' and are connected in parallel with the other connectors which carry these signals. The pinout assignments for the J3 connector are shown in Table 4-1. Table 4-1 also shows the corresponding P2 pinout for these signals.

4.4 J4 PDC CONNECTOR

The J4 20 pin connector carries the PDC signals which can be used to drive the PC26V time display module. The pin assignments for the J4 connector are shown in Table 4-2. Table 4-2 also shows the corresponding P2 pinout for these signals.

4.5 PDC SIGNAL DESCRIPTION

The signals carried on the PDC (Peripheral Data Connector) are generally used to drive other Bancomm products which require decoded time such as the PC26V display module. These signals can, however, be used by the user for a variety of applications.

Decoded time is transmitted over the PDC once per second using the PDC ENABLE* and D0-D7 lines in a byte serial fashion (i.e. a burst of 9 bytes are sent) just after the 1PPS mark. The D0-D7 encoding is shown in Table 4-3. The lower nibble contains the BCD encoded time digit and the upper nibble determines which digit has been transmitted. The D0-D7 data lines are valid when PDC ENABLE* is low.

PC03V VMEbus TIME CODE PROCESSOR I/O PINOUTS		
J3	P2	SIGNAL DESCRIPTION
13	C1	Time Code Channel 1 Input
12	C2	Time Code Channel 2 Input
11	C3	Time Code Channel 3 Input
10	C4	Time Code Channel 4 Input
9	C5	External Event Trigger Input
8	C6	Heartbeat Pulse Output
7	C7	Internal Gate Output
6	C8	Time Coincidence Strobe #2 Output
5	C9	Time Coincidence Strobe #1 Output
4	C29	1 Pulse Per Second (PPS) Output
17 - 25	A1 - A29	Ground

Table 4-1: J3 and P2 I/O Connector Pinouts

EACH CYCLE is a TTL representation of the time code carrier (high during positive half cycles, low during negative half cycles).

HIGH CYCLE* is a TTL signal that is low during a portion of a positive high amplitude cycle.

1PPS is a TTL signal, 1 carrier cycle wide, whose rising edge occurs on-time.

FSYNC* is a TTL signal, 1 carrier cycle wide, whose falling edge occurs once per frame at the on-time mark.

PC03V VMEbus TIME CODE PROCESSOR PDC PINOUTS		
J4	P2	SIGNAL DESCRIPTION
1	C23	Ground
2	A23	PDC ENABLE*
3	C24	D0
4	A24	D1
5	C25	D2
6	A25	D3
7	C26	D4
8	A26	D5
9	C27	D6
10	A27	D7
11	C28	EACH CYCLE
12	A28	HIGH CYCLE*
13	C29	1PPS
14-16	---	Not Used
17	C31	FSYNC*
18	A31	Ground
19	C32	+5 VDC
20	A32	+5 VDC

Table 4-2: PDC Connector Pinouts

PDC DATA FORMAT				
D7	D6	D5	D4	D3 - D0 (BCD)
0	0	0	0	Days Hundreds
0	0	0	1	Days Tens
0	0	1	0	Days Units
0	0	1	1	Hours Tens
0	1	0	0	Hours Units
0	1	0	1	Minutes Tens
0	1	1	0	Minutes Units
0	1	1	1	Seconds Tens
1	0	0	0	Seconds Units

Table 4-3: PDC Data Format

CHAPTER FIVE
THEORY OF OPERATION

5.0 GENERAL

This section describes the theory of operation for the PC03V Module. Reference the PC03V Schematic Diagram (11490).

5.1 TIME CODE READER

The heart of the PC03V Module is the circuitry used to convert the serial modulated time code signal into the parallel BCD format which can be read over the VMEbus.

One of four channels of time code is selected for decoding through an analog switch. The output of this switch is passed to an automatic gain control (AGC) circuit to equalize the level of the signal. The equalized signal drives two slicers; one slicer generates a TTL level 'each cycle' clock (high for the positive half of the cycle and low for the negative half of the cycle); the other slicer generates a TTL level 'high cycle' signal which is low for a portion of the positive high amplitude cycle. These two signals drive the digital time code reader circuitry which consists of the U10 and U16 PLD's, the U6 EPROM, and the U11 Z8 microcontroller.

The Z8 performs validation of the incoming decoded major time and writes this time to a bank of latches inside the Xilinx Logic Cell Array (LCA) and to the PDC connector.

5.2 TIME CAPTURE AND MINOR TIME COUNTERS

The minor time (subseconds) is generated by six decade counters which count either carrier cycles or the 1 MHz PLL clock. These counters are synchronized to the time code 1PPS by a signal generated by the time code decoder. When the counters roll-over to 0, the major time is clocked into a second set of latches.

When a time capture source is activated, all time of day digits (days - microseconds) are clocked into a set of latches which can be read over the VMEbus. Special circuitry is employed to assure that the time is not latched during a counter transition. If the time capture coincides with a counter transition then the time capture is held off until the counter outputs settle.

5.3 HEARTBEAT AND STROBES

The programmable interval heartbeat pulse is generated by the 82C54 CTC which is driven by the carrier or 1MHz PLL clock. This counter can be synchronized to the 1PPS through it's GATE input.

The time coincidence strobes are generated by a bank of comparaters which compares the decoded time to the time stored in the strobe registers (STR1W3-1 and STR2W3-1). The interval gate is generated by a flip-flop which is set when strobe #1 is activated and reset when strobe #2 is activated.

5.4 VMEbus INTERFACE

The VMEbus interface consists of the usual assortment of bus transceivers, buffers, and decoders commonly found on any microprocessor based system. Support for the interface is provided by the VME 2000 Slave Module Interface device from PLX and the MC68153 Bus Interrupter Module from Motorola.

CHAPTER SIX
PROGRAMMING EXAMPLES

6.0 GENERAL

This section provides programming examples which illustrate the use of the capabilities of the PC03V. Examples are shown in a simple pseudo-code. The following two functions are used to indicate VMEbus A16:D16 reads from and writes to the PC03V registers.

```
Read(Reg)              /* returns data at address offset Reg */
Write(Data, Reg)       /* writes $Data to address offset Reg */
```

The prefix '$' denotes a hexadecimal value.

6.1 CAPTURING AND READING TIME

This example shows how to capture time using the CAPTR register then reads the time into the array 'TimeArray'. The PC03V is configured for IRIG B, forward, microsecond resolution, channel 1.

```
Write($00,CR0);                 /* Configure CR0 for IRIG B   */
                                /* Forward, PLL clock, Ch 1   */
Write($0000,CR1);               /* Disable Ints, disable  */
                                /* secondary capture source   */
Dummy = Read(CAPTR);            /* Capture time           */
TimeArray[0] = Read(TIME0);     /* Read 4 time registers      */
TimeArray[1] = Read(TIME1);
TimeArray[2] = Read(TIME2);
TimeArray[3] = Read(TIME3);
```

6.2 EXTERNAL EVENT TRIGGER

This example shows how to setup the control registers and BIM registers to use the Event Trigger to capture time and generate an interrupt.

```
Write($00,CR0);         /* Configure CR0 as above          */
Write($0001,CR1);       /* Disable Ints, enable ext        */
                        /* event for time capture          */
Write($11,BIMCR0);      /* Enable BIM Int on level 1       */
Write(Vector,BIMV0);    /* Set interrupt vector data       */
Write($0009,CR1);       /* Enable Int Source 0         */
Dummy = Read(RELFR);    /* Release Capture Lockout         */

/* Wait for Interrupt          */
/* Interrupt Service Routine   */
```

```
TimeArray[0] := Read(TIME0);
      etc.
Dummy = Read(RELFR);       /* Release Capture Lockout          */
```

6.3 TIME COINCIDENCE STROBES

This example illustrates the use of the two strobes and the interval gate without using the interrupts.

```
Write($00,CR0)             /* Configure CR0 as above           */
Write($0C00,CR1)           /* Strobes are active low,          */
                           /* Interval gate is active high     */
                           /* Interrupts are disabled          */
Write(Strobe1[1],STR1W1);  /* Write Strobe #1 data to regs     */
Write(Strobe1[2],STR1W2);
Write(Strobe1[3],STR1W3);

/* Write Strobe #2 data    */

Dummy = Read(CLRIG);       /* Clear Interval Gate              */
```

6.4 PROGRAMMABLE INTERVAL HEARTBEAT

The first example shows how to use the heartbeat and synchronize it to the 1PPS. The heartbeat will repeat every 100 microseconds and is enabled to capture time. Using CTC Mode 5 the heartbeat repeats every N + 1 (99 + 1) counts.

```
Write($00,CR0);            /* Configure CR0 as above           */
Write($2005,CR1);          /* Sync Heartbeat, enable capture   */
Write($3A,CTCCR);          /* CTC Counter 0 Mode 5             */
Write(99,CTC0);            /* CTC Count Least Significant Byte */
Write(0,CTC0);             /* CTC Count Most Significant Byte  */
```

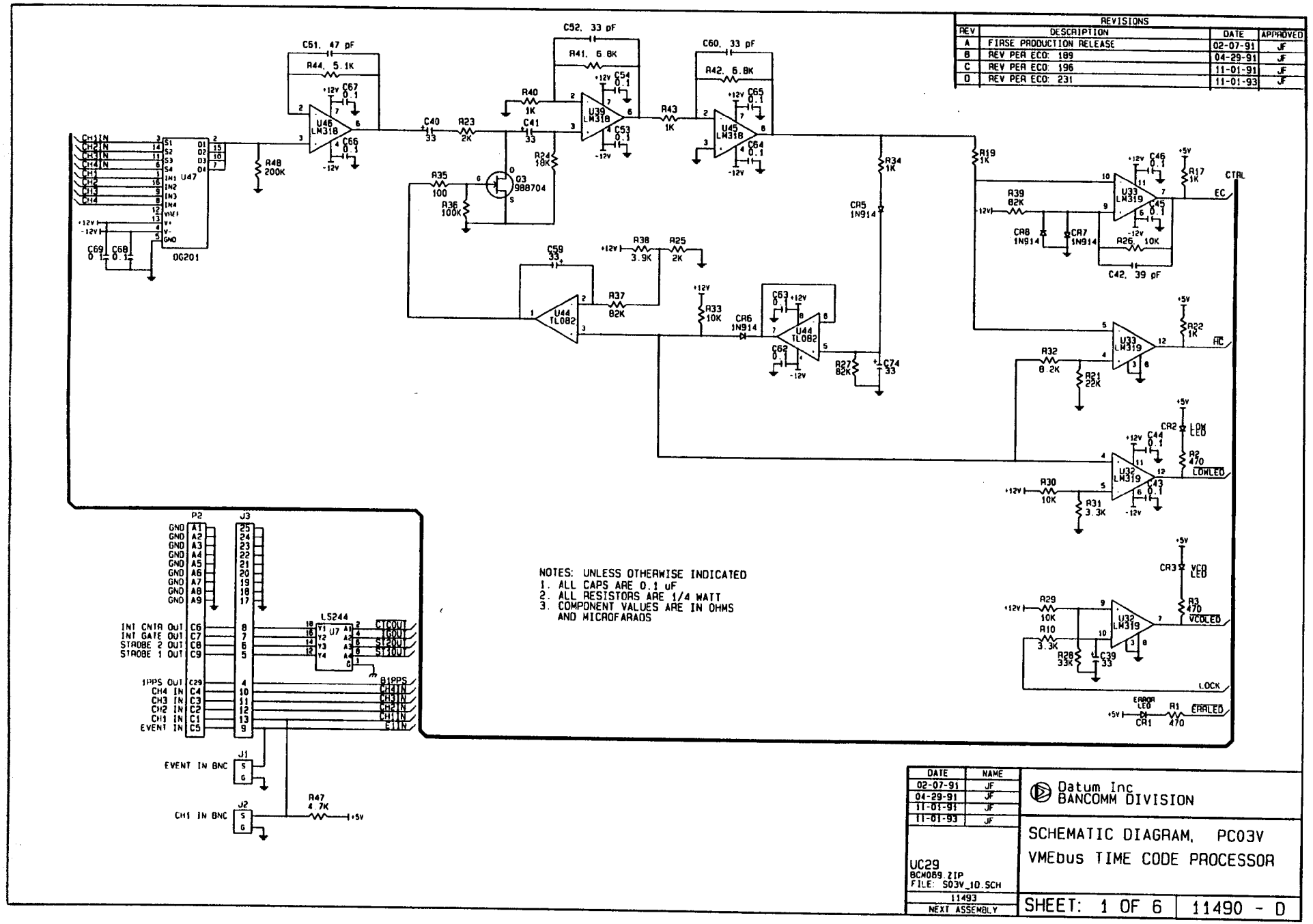
This example show how to use the heartbeat without 1PPS synchronization. The heartbeat will repeat every 380 microseconds and is enabled to capture time and generate an interrupt. Using CTC Mode 2 the heartbeat repeats every N (380) counts.

```
Write($00,CR0);            /* Configure CR0 as above           */
Write($0005,CR1);          /* No Sync, enable capture, disable int */
Write($13,BIMCR1);         /* Enable BIM Int on level 3        */
Write(Vector,BIMV1);       /* Set interrupt vector data        */
Write($34,CTCCR);          /* CTC Counter 0 Mode 2             */
Write(124,CTC0);           /* CTC Count LSB                    */
Write(1,CTC0);             /* CTC Count MSB                    */
Write($0015,CR1);          /* Enable interrupt source 1        */
```

CHAPTER SEVEN
DRAWINGS

7.0 GENERAL

This section contains the schematic diagrams, assembly drawings, and parts lists for the PC03V VMEbus Time Code Processor Module.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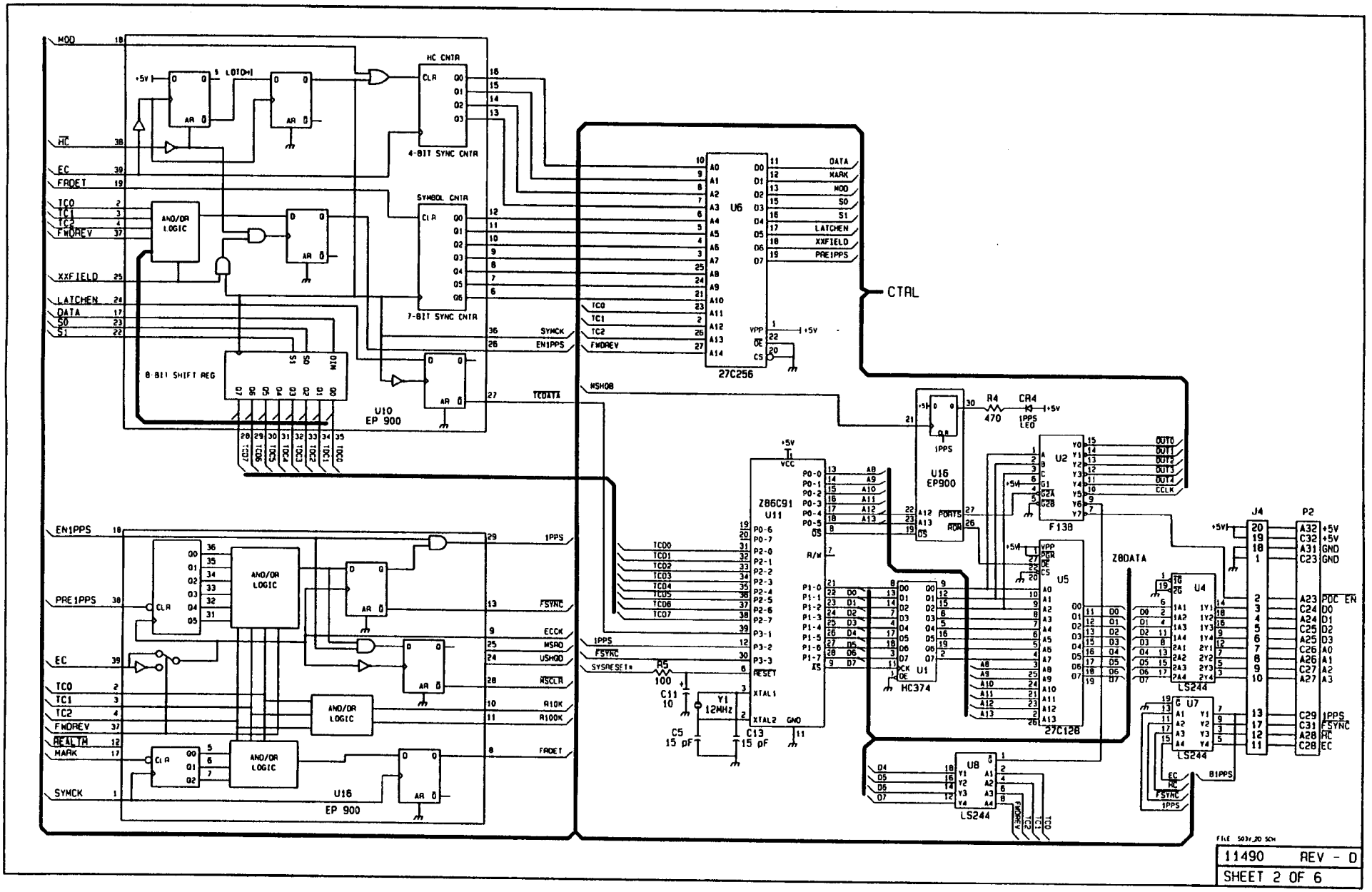
B | REV PER ECO: 189 | 04-29-91 | JF
C | REV PER ECO: 196 | 11-01-91 | JF
D | REV PER ECO: 231 | 11-01-93 | JF
NOTES: UNLESS OTHERWISE INDICATED
1. ALL CAPS ARE 0.1 uF
2. ALL RESISTORS ARE 1/4 WATT
3. COMPONENT VALUES ARE IN OHMS AND MICROFARADS
Datum Inc
BANCOMM DIVISION
SCHEMATIC DIAGRAM, PC03V
VMEbus TIME CODE PROCESSOR
UC29
BCM089.ZIP
FILE: S03V_ID.SCH
11493
NEXT ASSEMBLY
SHEET: 1 OF 6
11490 - D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EC
FRDET
TC0
TC1
TC2
FWDREV
XXFIELD
LATCHEN
DATA
S0
S1
HC CNTR
4-BIT SYNC CNTR
SYMBOL CNTR
7-BIT SYNC CNTR
AND/OR LOGIC
8-BIT SHIFT REG
U10
EP 900
SYMCK
EN1PPS
TCDATA
CTRL
U6
27C256
MSH08
R4
470
CR4
1PPS LED
U16
EP900
Z86C91
U11
U2
F138
U5
27C128
U1
HC374
Z80DATA
U4
LS244
U7
U8
J4
P2
R5
100
C11
10
C5
15 pF
C13
15 pF
Y1
12MHz
EN1PPS
PRE1PPS
REALTM
MARK
SYMCK
1PPS
FSYNC
ECCK
MSRQ
USHOD
RSCLR
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A100K
FRDET
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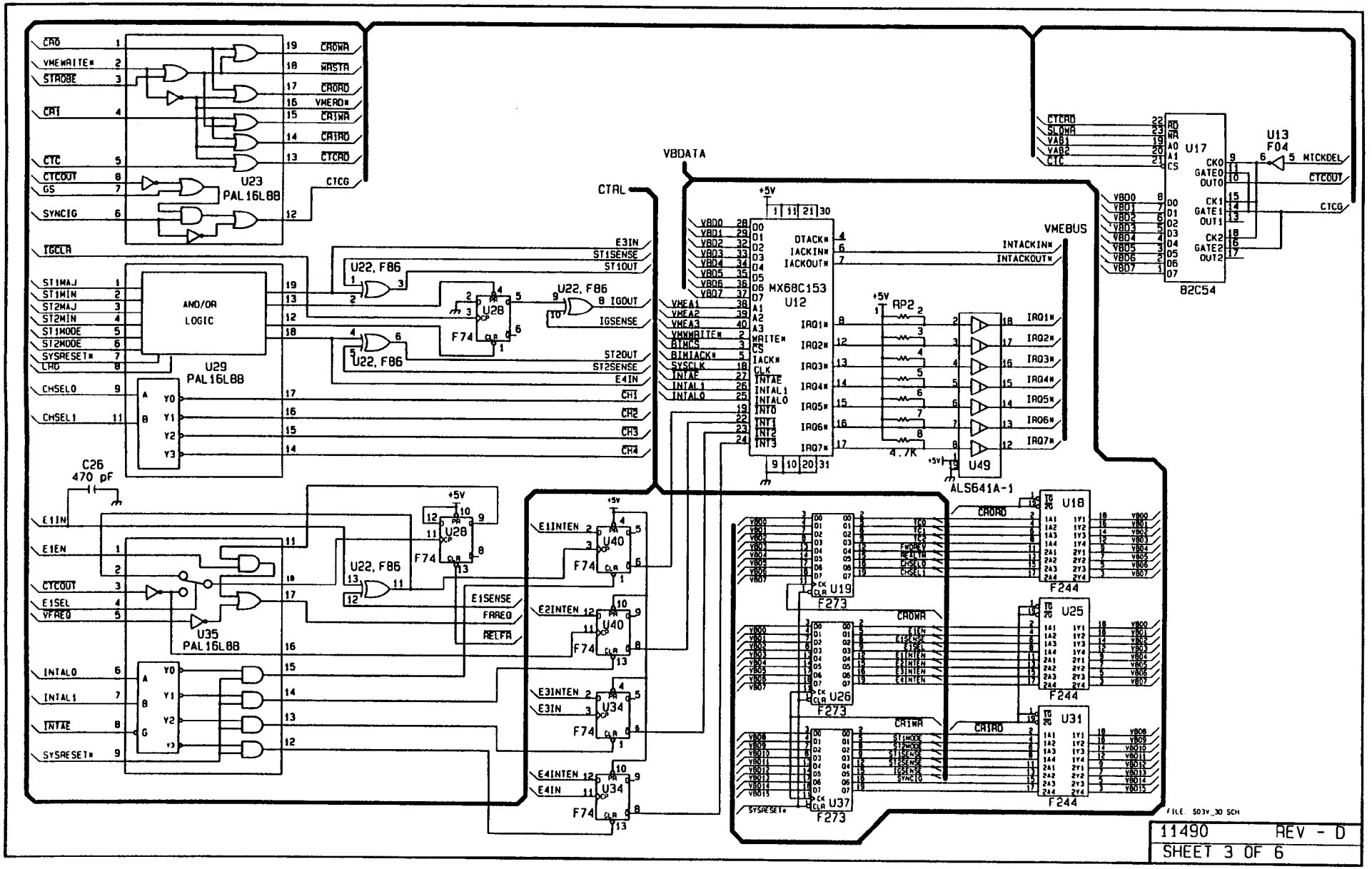
EP 900
SYSRESET*
11490 REV - D
SHEET 2 OF 6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PAL16L88
U29
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U35
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AND/OR
LOGIC
MX68C153
U12
VMEBUS
82C54
U17
U13
F04
ALS641A-1
U49
RP2
4.7K
C26
470 pF
VBDATA
CTRL
U18
U19
U25
U26
U31
U37
F273
F244
U22, F86
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U40
U34
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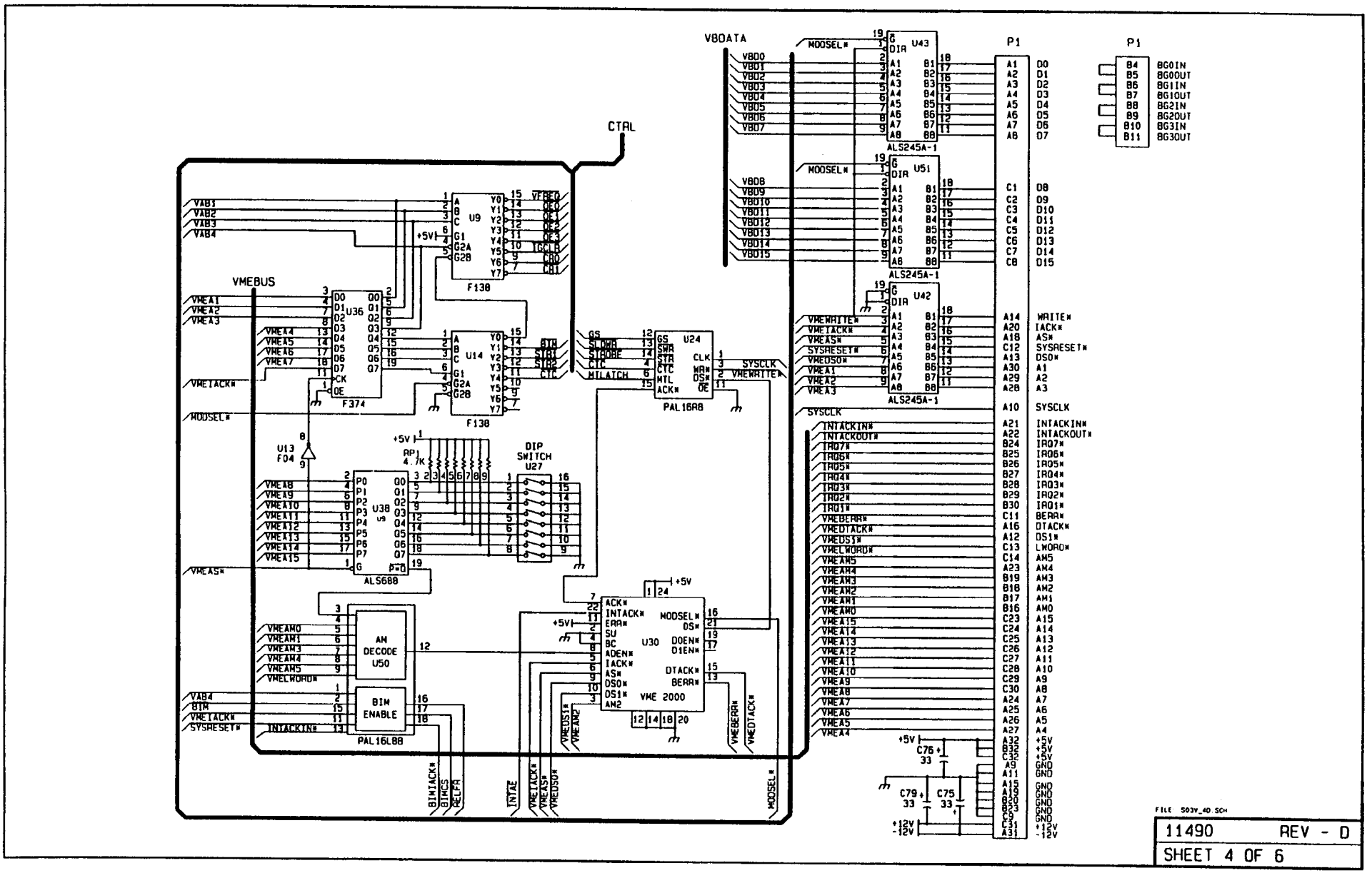
REV - D
SHEET 3 OF 6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VMEBUS
P1
P1
U43
U51
U42
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U9
F138
U36
F374
U14
F138
U24
PAL16R8
U13
F04
RP1
4.7K
DIP
SWITCH
U27
U38
ALS688
AM
DECODE
U50
BIN
ENABLE
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U30
VME 2000
C76
33
C79
33
C75
33
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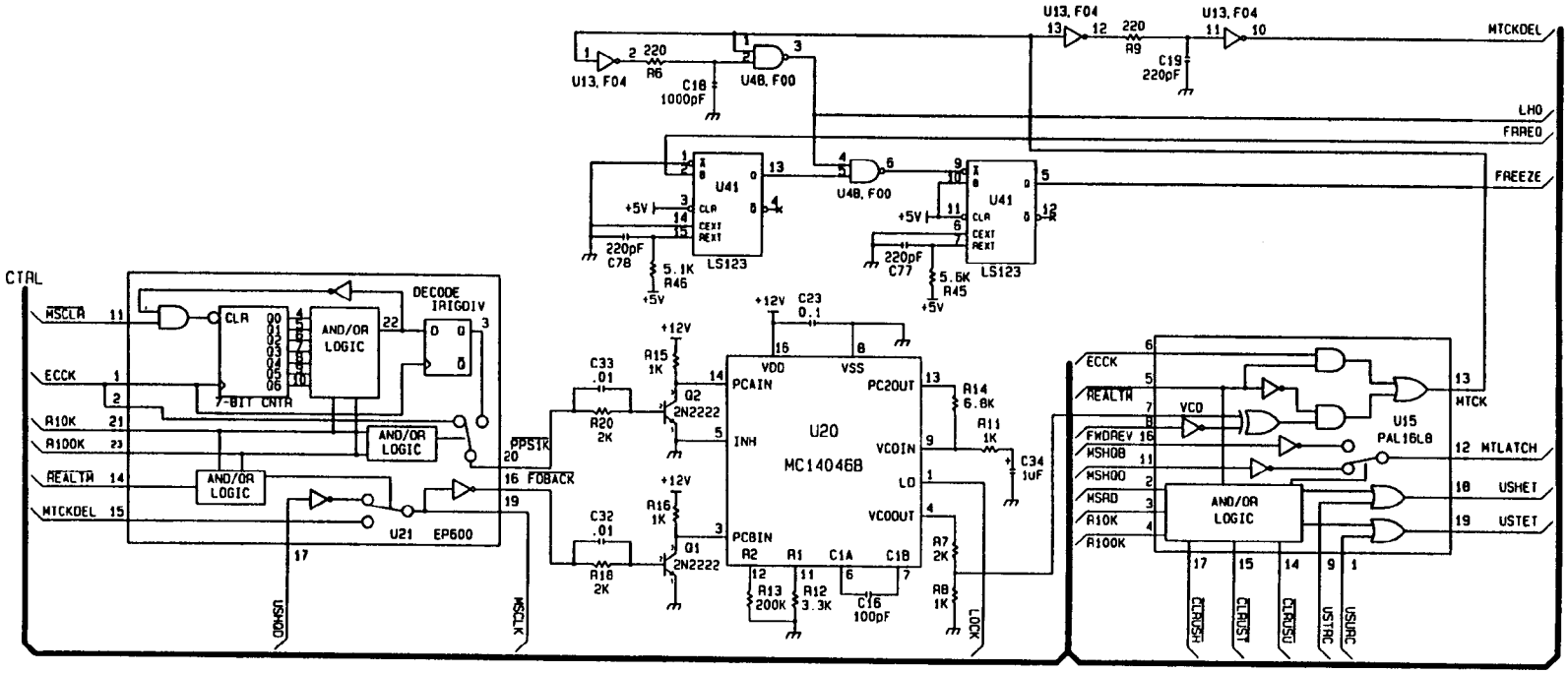
SHEET 4 OF 6



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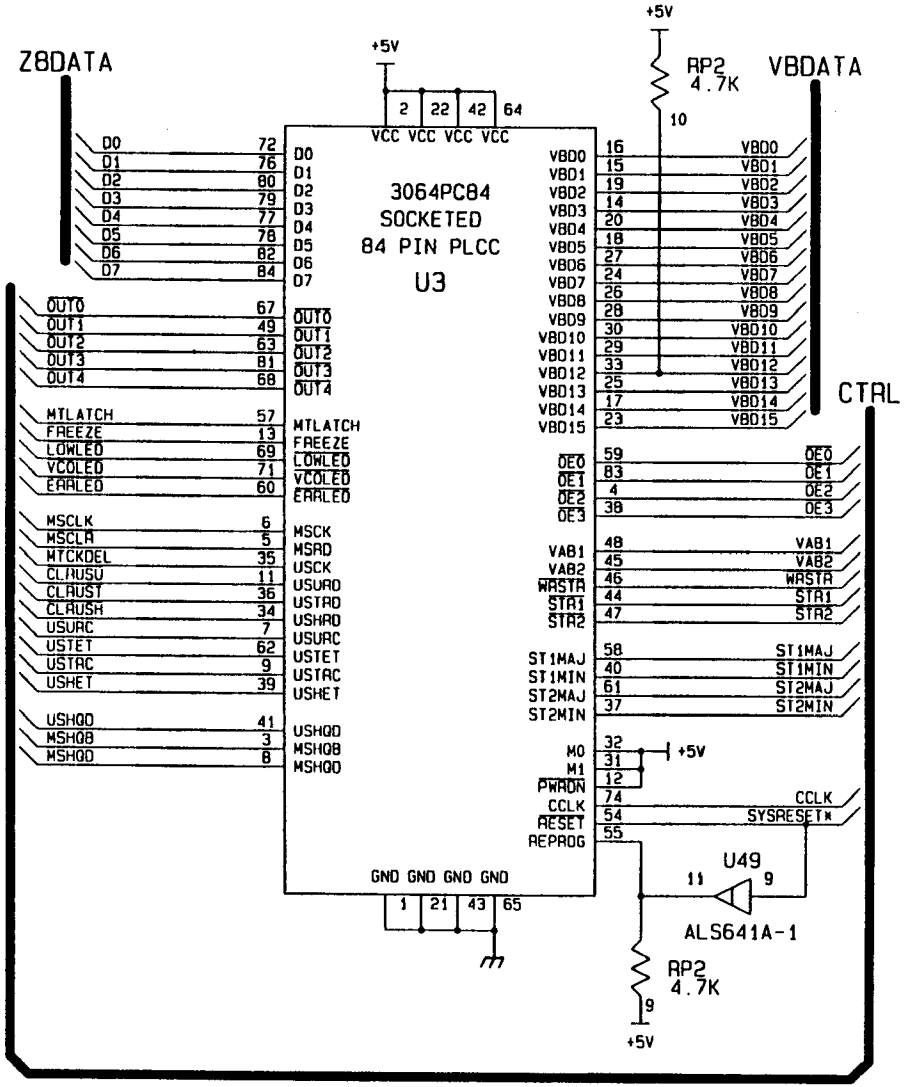

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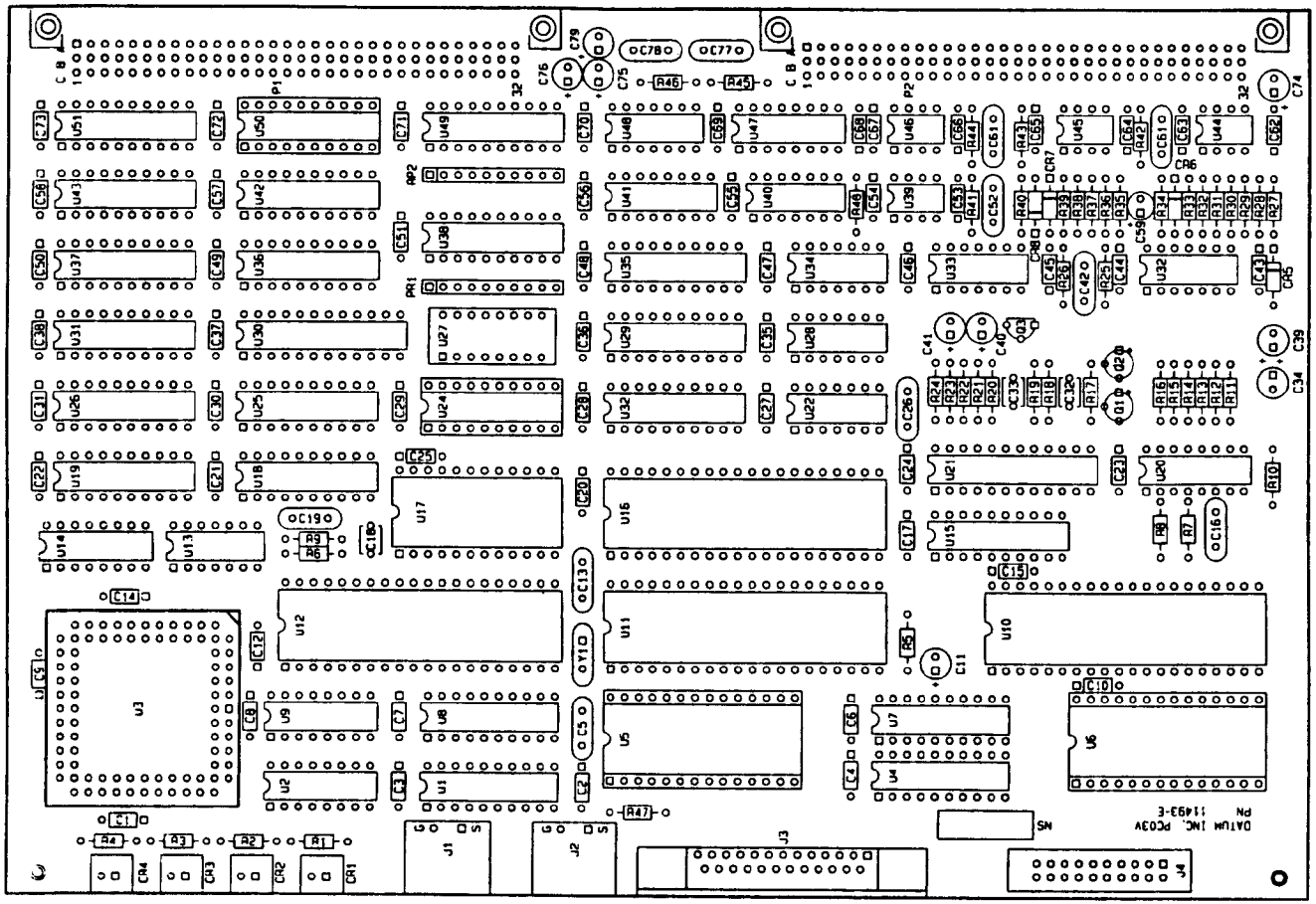

REVISIONS			
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B	REV PER ECO: 189	04-29-91	J.F.
C	REV PER ECO: 196	11-01-91	J.F.
D	REV PER ECO: 231	11-01-93	J.F.
E	REV PER ECO: 280	12-16-95	M.B.

UC29 BCM069.ZIP FILE: A03V_1E.SCH	Datum Inc BANCOMM DIVISION	
DRN BY: JWL	ASSY DIAG, PC03V VMEbus TIME CODE PROCESSOR	
DATE: Dec 16, 1995		
CHECKED BY:	SHEET: 1 OF 3	11493-E

Assembly, Parts Listing
PC03V VMEbus Time Code Processor

Ref: Drawing No. 11493 E
Ref: UC 029
Nov 16, 1995

OPT	BC P/N	MANF P/N	MANUFACTURE	VALUE	DESCRIPTION	QTY#	REF DESIG.
	1501101	CD15FD101J03	CDE	100 PF, 500V	DIPPED MICA CAPACITOR	1.00	C16
	1501150	CM05CD150J03	CDE	15 PF, 500V	DIPPED MICA CAPACITOR	2.00	C5,13
	1501221	SCDM10FD221J	ARCO	220 PF, 500V	DIPPED MICA CAPACITOR	3.00	C19,77,78
	1501330	CM05ED330J03	ARCO	33 PF, 500V	DIPPED MICA CAPACITOR	2.00	C52,60
	1501390	CM05ED390J03	ARCO	39 PF, 500V	DIPPED MICA CAPACITOR	1.00	C42
	1501470	CM05ED470J03	ARCO	47 PF, 500V	DIPPED MICA CAPACITOR	1.00	C61
	1501471	CD15FD471J03	CDE	470 PF, 500V	DIPPED MICA CAPACITOR	1.00	C26
	1503336	336RMR025M	IC	33 MF, 35V	ALUMINUM ELECTROLYTIC CAP.	8.00	C39-41,59,74-76,79
	1504105	196D105X9035HA1	SPRAGUE	1.0 MF, 35V	TANTALUM CAP, RADIAL LEADS	1.00	C34
	1506102	SR211C102KAA	AVX	1000 PF, 50V	MONO CERAMIC CAPACITOR .2 R/L	1.00	C18
	1506103	SR211C103KAA	AVX	0.01 MF, 100V	MONO CERAMIC CAPACITOR .2 R/L	2.00	C32,33
	1515104	MD015E104MAA	AVX/67349	0.1 MF, 50V	DIP GUARD CAPACITOR	19.0(	C1-4,6-10,12,14,15,17,20-25---
	1515104	MD015E104MAA	AVX/67349	0.1 MF, 50V	DIP GUARD CAPACITOR	36.0(	C27-31,35-38,43-51,53-58,62-73
	1701029	11492E	BANCOMM DIV, DATUM	PC03V Processor	PRINTED CIRCUIT BOARD	1.00	PCB1
	2101003	31-221	AMPHENOL	50 OHM	FRONT MNT BNC BULKHEAD RECEP.	2.00	J1,2
	2104001	913346	ERNI	96 POS	DIN CONNECTOR, MALE	2.00	P1,2
	2111020	3592-6002	3M	20 POS	CONTACT HEADER	1.00	J4
	2124225	869448-1	AMP	25 PIN	'D' SKT, .318 RTANG PCMNT B/L	1.00	J3
	2150020	10620-01-445	ANDON/SPECIRA	20 POS	DIP SOCKET	2.00	REF: U24,50
	2150028	10628-01-445	ANDON/SPECIRA	28 POS	DIP SOCKET	2.00	REF: U5,6
	2150040	10640-01-445	ANDON/SPECIRA	40 POS	DIP SOCKET	4.00	REF: U10,11,12,16
	2152084	PLCC-84-AGN	ADAM TECH	84 POS	PLCC REC CHIP CARRIER	1.00	REF: U3
	2302004	DS-1200	SEIKO	12 MHz	CRYSTAL	1.00	Y1
	2401600	10775D	BANCOMM DIV, DATUM		PC03V READER FT. PANEL	1.00	BKT1
	2404600	VME-6U-1450	PHILLIPS COMPONENTS		VME EXTRACTOR HANDLES KIT	1.00	BKT1
	2802002	3341-1S	3M		JACK SCREW KIT	1.00	BKT1
	3701031	550-2206	DIALIGHT		GREEN LED, RT ANGLE PC MOUNT	2.00	CR3,4
	3701033	550-2406	DIALIGHT		RED LED, RT ANGLE PC MOUNT	2.00	CR1,2
	4701101	RC07GF101J	ALLEN BRADLEY	100 OHM,1/4W	FIXED RESISTOR	2.00	R5,35
	4701102	RC07GF102J	ALLEN BRADLEY	1 K OHM,1/4W	FIXED RESISTOR	10.0(	R8,11,15-17,19,22,34,40,43
	4701103	RC07GF103J	ALLEN BRADLEY	10 K OHM,1/4W	FIXED RESISTOR	4.00	R26,29,30,33
	4701104	RC07GF104J	ALLEN BRADLEY	100 K OHM,1/4W	FIXED RESISTOR	1.00	R36
	4701183	RC07GF183J	ALLEN BRADLEY	18 K OHM,1/4W	FIXED RESISTOR	1.00	R24
	4701202	RC07GF202J	ALLEN BRADLEY	2 K OHM,1/4W	FIXED RESISTOR	5.00	R7,18,20,23,25,
	4701204	RC07GF204J	ALLEN BRADLEY	200 K OHM,1/4W	FIXED RESISTOR	2.00	R13,48
	4701221	RC07GF221J	ALLEN BRADLEY	220 OHM,1/4W	FIXED RESISTOR	2.00	R6,9
	4701223	RC07GF223J	ALLEN BRADLEY	22 K OHM,1/4W	FIXED RESISTOR	1.00	R21
	4701332	RC07GF332J	ALLEN BRADLEY	3.3 K OHM,1/4W	FIXED RESISTOR	3.00	R10,12,31
	4701333	RC07GF333J	ALLEN BRADLEY	33 K OHM,1/4W	FIXED RESISTOR	1.00	R28
	4701392	RC07GF392J	ALLEN BRADLEY	3.9 K OHM,1/4W	FIXED RESISTOR	1.00	R38
	4701471	RC07GF471J	ALLEN BRADLEY	470 OHM,1/4W	FIXED RESISTOR	4.00	R1-4
	4701472	RC07GF472J	ALLEN BRADLEY	4.7 K OHM,1/4W	FIXED RESISTOR	1.00	R47
	4701512	RC07GF512J	ALLEN BRADLEY	5.1 K OHM,1/4W	FIXED RESISTOR	2.00	R44,46
	4701562	RC07GF562J	ALLEN BRADLEY	5.6 K OHM,1/4W	FIXED RESISTOR	1.00	R45
	4701682	RC07GF682J	ALLEN BRADLEY	6.8 K OHM,1/4W	FIXED RESISTOR	3.00	R14,41,42
	4701822	RC07GF822J	ALLEN BRADLEY	8.2 K OHM,1/4W	FIXED RESISTOR	1.00	R32
	4701823	RC07GF823J	ALLEN BRADLEY	82 K OHM,1/4W	FIXED RESISTOR	3.00	R27,37,39
	4705472	710A472	ALLEN BRADLEY	4.7 K OHM,1/8W	C-SIP RESISTORS, 10 PIN 'X'	2.00	RP1,2
	4801002	2N2222			NPN SWITCHING/AMPLIFIER (TO18)	2.00	Q1,2
	4803001	IN914			SILICON DIODE	4.00	CR5-8
	4807001	988704	DATUM INC	T092 PACKAGE	N-CHANNEL J-FET	1.00	Q3
	5108002	76SB08	GRAYHILL		8PST DIP SWITCH	1.00	U27
	9002800	74F00	NATIONAL	14P DIP PKG	QUAD 2-INPUT NAND GATE	1.00	U48
	9002802	74F04	NATIONAL	14P DIP PKG	HEX INVERTOR	1.00	U13
	9004832	74F138	NATIONAL	16P DIP PKG	1-OF-8 DECODER/DEMUX	3.00	U2,9,14
	9006658	74HC374	MOTOROLA	20P DIP PKG	OCTAL D FLIP FLOP	1.00	U1
	9006818	74F74	NATIONAL	14P DIP PKG	DUAL D FLIP FLOP	3.00	U28,34,40
	9006858	MM74F374N	NATIONAL	20P DIP PKG	OCTAL D FLIP FLOP	1.00	U36

OPT	BC P/N	MANF P/N	MANUFACTURE	VALUE	DESCRIPTION	QTY#	REF DESIG.
	9007823	74F86	NATIONAL	14P DIP PKG	QUAD 2-INPUT EXCLUSIVE OR GATE	1.00	U22
	9011127	74LS123	FAIRCHILD	16P DIP PKG	DUAL MULTIVIBRATOR	1.00	U41
	9013851	74F273	NATIONAL	20P DIP PKG	8 BIT SHIFT REGISTER	3.00	U19,26,37
	9015940	SN74ALS688N	TI	20P DIP PKG	8 BIT MAGNITUDE COMPARATOR	1.00	U38
	9102001	Z86C9112PEC	ZILOG	40P DIP PKG .6W	Z8 MICROCONTROLLER	1.00	REF: U11 (SKT)
	9103008	82C54	AMD	24P DIP PKG .6W	CMOS COUNTER TIMER	1.00	U17
	9103031	MX68C153	MACRONIX	40P DIP PKG .6W	CMOS BUS INTERRUPT MODULE	1.00	REF: U12 (SKT)
	9201025	DG201BK	INTERSIL	16P DIP PKG	ANALOG SWITCH	1.00	U47
	9207015	74LS244	FAIRCHILD	20P DIP PKG	OCTAL BUFFER/LINE DRIVER, 3S	3.00	U4,7,8
	9207815	74F244	NATIONAL	20P DIP PKG	OCTAL BUFFER/LINE DRIVER	3.00	U18,25,31
	9207920	SN74ALS245A-1N	TI	20P DIP PKG	OCTAL BUS TRANSCEIVER	3.00	U42,43,51
	9207925	SN74ALS641A-1N	TI	20P DIP PKG	OCTAL BUS TRANSCEIVER	1.00	U49
	9211001	VME2000-45	PLX TECHONLOGY	24P DIP	VME SLAVE INTERFACE	1.00	U30
	9303015	LM319N	NATIONAL	14P DIP PKG	HIGH SPEED DUAL COMPARATOR	2.00	U32,33
	9306025	LM318N	NATIONAL	08P DIP PKG	OP AMP, 8 PIN DIP	3.00	U39,45,46
	9306035	TL082	TI	08P DIP PKG	DUAL BIPOLAR JFET OP AMP	1.00	U44
	9307020	MC14046B	MOTOROLA	16P DIP PKG	PHASE LOCK LOOP	1.00	U20
	9405001	EP600DC-3	ALTERA	24P DIP PKG .3W	EPLD	1.00	U21
	9405010	EP900DC-3	ALTERA	40P DIP PKG .6W	PAL	2.00	REF: U10,16 (SKT)
	9405015	PAL16L8B	MMI	20P DIP PKG .3W	PAL	5.00	U15,23,29,35,50
	9405030	PAL16R8BCN	MMI	20P DIP PKG .3W	PAL 35 NS	1.00	REF: U24 (SKT)
	9405050	XC3064-50PC84C	XILINX	84P PLCC PKG	PLD	1.00	REF: U3 (SKT)
	9406040	27C256	VARIOUS	28P DIP PKG .6W	32 K BYTE, CMOS EPROM	1.00	REF: U6 (SKT)
	9406308	27C128		28P DIP PKG .6W	16 K BYTE EPROM	1.00	REF: U5 (SKT)